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Interfacing ISP1160x to Fujitsu® SPARClite® RISC Processor

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Application Note

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Note: ISP1160x denotes any Philips embedded USB host controller whose name starts with 'ISP1160'; this includes ISP1160A, ISP1160A1, and any future derivatives.

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Note: ISP1160x denotes any Philips embedded USB host controller whose name starts with 'ISP1160'; this includes ISP1160A, ISP1160A1, and any future derivatives.

1. Overview

When the ISP1160x is integrated into a personal digital assistant (PDA) or handheld personal computer (HPC), it is usually connected to the external bus interface of a Reduced Instruction Set Computer (RISC) processor. This application note presents some of the important issues in such a design, using a concrete example of the Fujitsu SPARClite RISC.

2. ISP1160x Processor Interface Signals

The processor bus interface of the ISP1160x is designed for a simple direct connection with a RISC processor. The data transfer can be done in the programmed I/O (PIO) or direct memory access (DMA) mode. The estimated maximum data transfer rate on the generic processor bus of the ISP1160x is approximately 15 Mbyte/s. This is based on an ISP1160x internal clock frequency value of 48 MHz. To achieve the maximum data transfer rate on the host processor bus, the ISP1160x contains a ping pong structured RAM that allows alternative access from the RISC processor or from the internal Host Controller. The Host Controller uses 2 kbytes of the ping memory and 2 kbytes of the pong memory in its allocated memory.

The main ISP1160x signals to consider when connecting to a Fujitsu SPARClite RISC processor are:

- A 16-bit data bus: (D[15:0]) for the ISP1160x. The ISP1160x is "little endian" compatible.
- An address line (A0), which is necessary for the complete addressing of the ISP1160x internal registers:
  - **A0 = 0**—Selects the Data Port of the Host Controller
  - **A0 = 1**—Selects the Command Port of the Host Controller
- A $\overline{\text{CS}}$ line used for selection of the ISP1160x in a certain address range of the host system. This input signal is active LOW.
- $\overline{\text{RD}}$ and $\overline{\text{WR}}$ are common read and write signals. These signals are active LOW.
- A set of DMA channel standard control lines: DREQ, $\overline{\text{DACK}}$ and EOT are used. Since the SPARClite processor does not contain a DMA controller, these signals will not be used in a minimal hardware implementation.
- An interrupt line INT, which is programmable as active on level or edge and HIGH or LOW.
- The CLKOUT signal has a maximum value of 48 MHz.
- The $\overline{\text{RESET}}$ signal is active LOW.

3. Fujitsu SPARClite

The SPARClite processor is part of the 32-bit RISC Fujitsu family.

The external bus interface of the SPARClite processor is a non-multiplexed address and data bus. It has a big-endian architecture. An internal programmable Chip Select logic and an on-chip address decoder allow easy interfacing to EPROM, DRAM (EDO/FPM), UART, or general ASIC without additional glue logic. The integrated DRAM controller can generate all the signals necessary to provide a direct interface to different types of memory; FPM and EDO DRAMS. The address decoder of the SPARClite processor can generate six programmable Chip Select signals. One of the CS0–CS5 signals will be asserted when the selected address matches the value programmed in the *Address Range Specifier Register*. The *Address Mask Register* is used to mask certain bits of the address.

To select the properties of each area, set certain values in the internal control registers:

- Bus size: 8, 16 or 32 bits can be independently set for each area, and is determined by the value of the *Bus Width/Cacheable Register* of the SPARClite processor.
- Number of wait cycles: can be independently set for each selected area by setting the *Wait States Specifier Register* of SPARClite.
- Setting the type of space: SRAM, DRAM and EPROM. The SPARClite processor will generate the necessary signals to control any of these types of memory.

Each addressed area of the SPARClite processor can be used only in the big endian mode. For correct data alignment, there must be matching data widths and matching endians. During the design phase of a system using SPARClite and ISP1160x, take extra care when developing schematics and software because the ISP1160x connection requires a 16-bit or little endian configuration of the selected memory area.

4. Considerations in Timing Diagrams and WAIT States

The following is a short study of the timing diagrams of the ISP1160x.

According to the ISP1160x datasheet specifications, a read cycle requires the following main timing parameters (the requirements of the write cycle are similar):

- t_{RL} = 33 ns ($\overline{RD}$ LOW pulse width—minimal value required by the ISP1160x),
- t_{RHRL} = 110 ns ($\overline{RD}$ HIGH to next $\overline{RD}$ LOW—minimal value required by the ISP1160x) and
- t_{RHDZ} = 3 ns ($\overline{RD}$ hold time, minimal value that can be expected from the ISP1160x).
- t_{RC} = 143 ns (will result as a sum of t_{RL} and t_{RHRL})
- t_{SHSL} = 300 ns (first $\overline{RD}$/$\overline{WR}$ after command).

For a detailed analysis of a timing diagram, consider the access of an ISP1160x internal register (for example, the Control Register of the Host Controller). It requires two phases: writing the address of the selected register into the Command Port; then only data transfer access (RD/WR) takes place.

The timing diagram in Figure 4-1 describes the two phases of accessing the ISP1160x:

- The first phase is accessing the ISP1160x Command (control) Port of the ISP1160x to write the address (index) of the data port that will be accessed. In this phase, $\overline{CS}$ is active. The data lines D[15:0] contain the desired address. The $\overline{WR}$ pulse will be activated and will latch the data. Note the value of t_{SHSL} that represents the minimum time required between occurrence of the first phase and the second phase. As an example of the Host Controller "Control Register", a value of 01H will be transferred during an $\overline{RD}$ operation and 81H during a $\overline{WR}$ operation.
- The second phase consists of the access (read or write) to the data port selected by the address latched in the previous phase. Two timing diagrams are combined again in this second phase: one for the read access and one for the write access. A series of $\overline{RD}$ and $\overline{WR}$ pulses are shown in the diagram to define the timing requirements between two consecutive accesses to the ISP1160: t_{RHRL}, t_{WHWL}, t_{RC}, t_{WC}, t_{RLDV}, as specified in the datasheet.

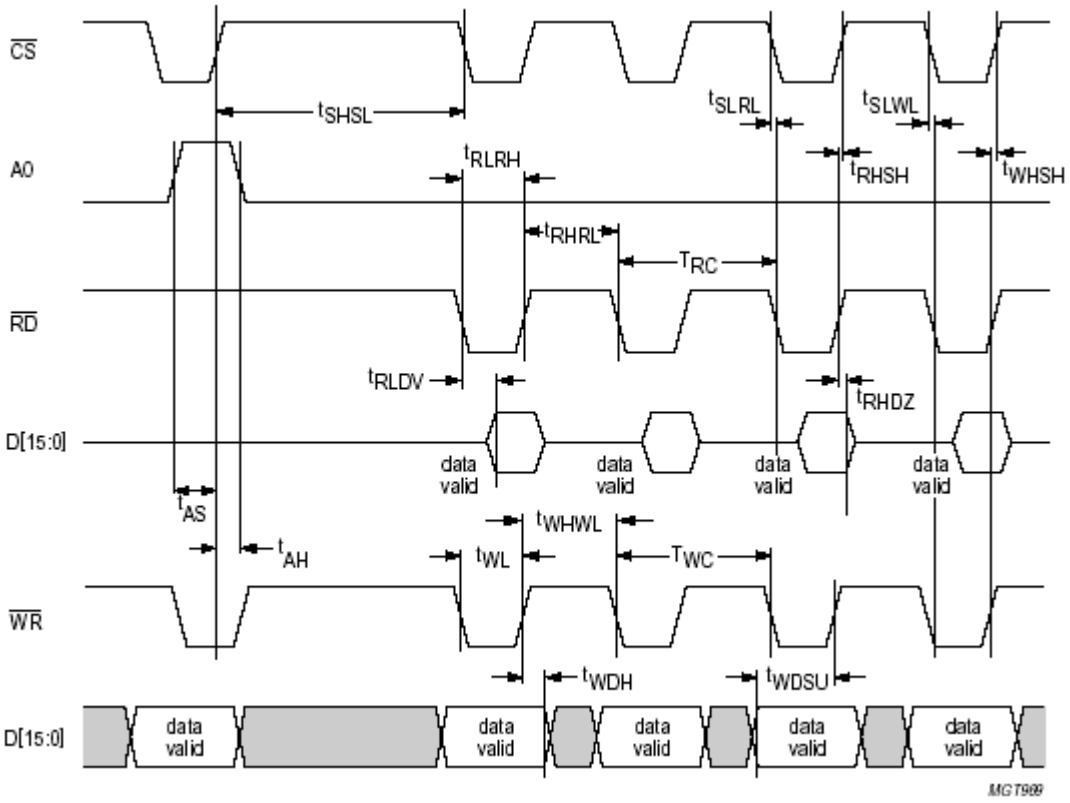


Figure 4-1: Programmed Interface Timing (16-bit Read/Write)

When the ISP1160x connection area is defined as SRAM, ISP1160x will operate correctly when the bus clock CKIO = 33 MHz. Timing measurements show that inserting wait-states in the standard bus cycles of SPARClite is unnecessary. Nevertheless, we will describe wait-state insertion, to cater for cases when faster bus cycles are used for accessing the ISP1160x.

Wait states insertion may be generally achieved using two solutions: hardware or software implementation. Both solutions will delay the rising edge of $\overline{RD}$ or $\overline{WR}$ to the next CKIO cycle and will determine an elongation of the $\overline{RD}$ or $\overline{WR}$ LOW pulse that can be calculated as:

t_w = W x T(CKIO); where: (W) is the number of wait states desired or selected.

T(CKIO) is the cycle length of CKIO.

Note: the value of t_{RHRL} will not be modified by the number of wait states inserted by any of the solutions mentioned earlier. The value of this parameter must be calculated and correctly adjusted according to the number and length of instructions executed by the SPARClite processor between two successive accesses to the ISP1160x. The "software solution" for wait-state insertion in a bus cycle is simple and is preferred in a minimal configuration, if additional wait states are necessary.

5. Using Interrupts

The ISP1160x generates an interrupt on the INT pin. This INT signal can be directly connected to any of the available IRQ signals of the SPARClite processor. The INT of the ISP1160x can be programmed as active on level or edge and HIGH or LOW, as specified in the *HcHardwareConfiguration Register*.

6. Schematic Diagram

The schematic diagram on the following page shows the connection of the ISP1160x to a Fujitsu SPARClite processor in a minimal hardware configuration. For a more detailed description on connecting the ISP1160x to a RISC processor and a study of each category of signals and timing diagrams, refer to the application note *Interfacing ISP1160x to Hitachi SH7709 RISC Processor*.

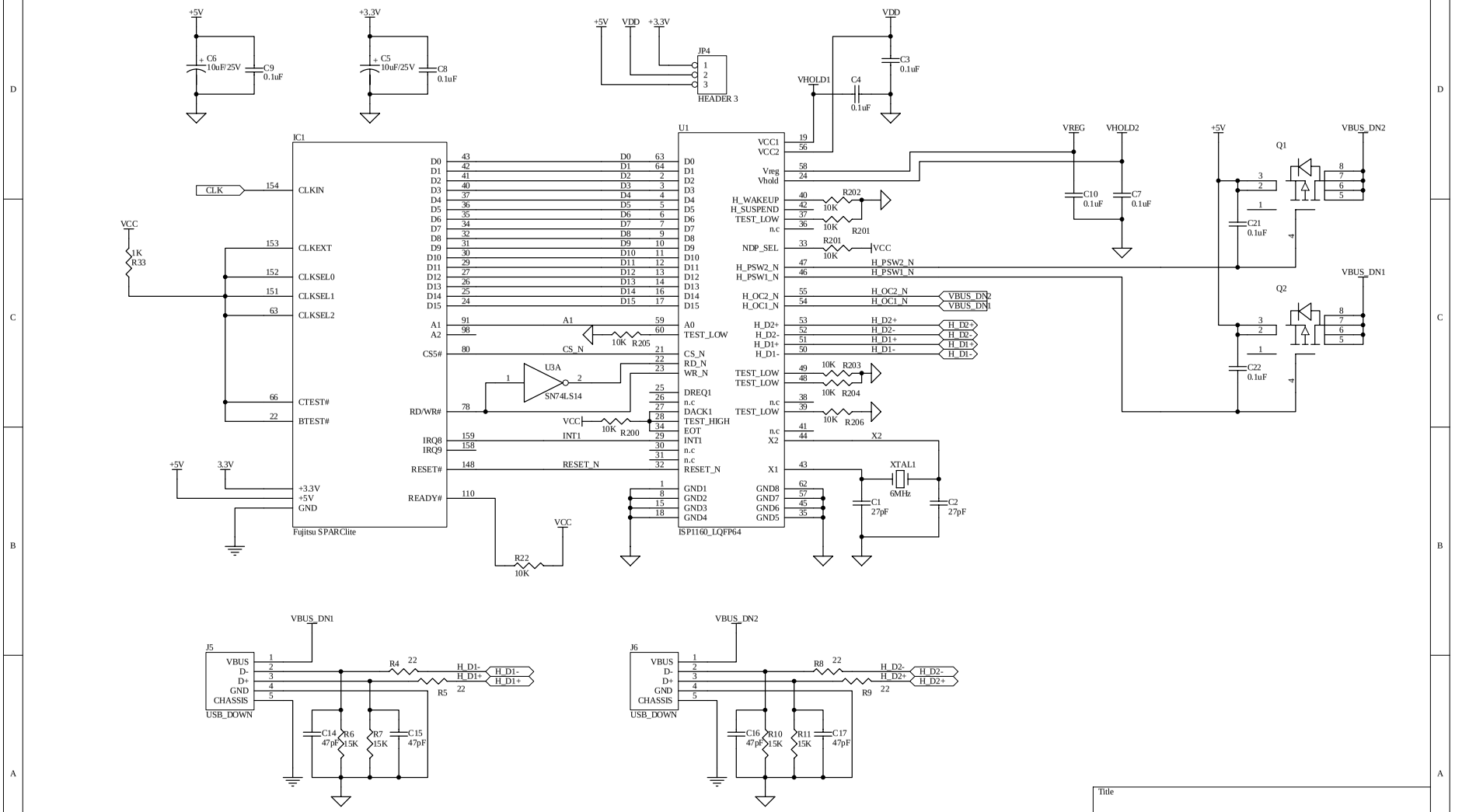
In this configuration, the ISP1160x is simply selected by CS5#, which is asserted according to the values programmed in the *Address Range Specifier Register* and the *Address Mask Register*.

To correctly access the ISP1160x, it is assumed that area 5 is programmed for the SRAM memory type for 16-bit accesses. Data lines D[15:0] of the SPARClite processor will be used in this configuration, and pull-up resistors must be connected to the data bus lines that are not used (D[31:16]); according to the SPARClite datasheet specifications. In this configuration, the $\overline{\text{RD}}$ input signal of the ISP1160x is generated by negating the $\overline{\text{RD}}/\overline{\text{WR}}$ signal generated by the SPARClite processor. Therefore, the $\overline{\text{RD}}$ input signal of the ISP1160x will be active most of the time as the SPARClite $\overline{\text{RD}}/\overline{\text{WR}}$ signal is HIGH during a read or idle cycle. This will not create any conflicts on the system data bus as the ISP1160x will enable its internal output buffers only when $\overline{\text{CS}}$ is also active in the same time.

Interrupt INT is arbitrarily connected to IRQ8 line of the SPARClite processor. The interrupt controller of the Fujitsu SPARClite processor allows independent setting of the interrupt trigger mode for each input, by programming its *Trigger Mode 0 and 1 Registers*. The ISP1160x also allows programming of polarity (LOW or HIGH) and the signaling mode (level or pulse) for the generated interrupt INT by correctly setting the bits of the *HcHardwareConfiguration* registers.

Input signals $\overline{\text{H\_OC1}}$ and $\overline{\text{H\_OC2}}$ are used by the ISP1160x to detect an overcurrent on the downstream facing ports. Since separate overcurrent detection and protection circuits are implemented for each downstream port in the ISP1160x, detection of overcurrent on a downstream port will cause power to be turned off at that port only. Connecting the voltages of the two downstream ports VBUS_DN1 and VBUS_DN2 to the $\overline{\text{H\_OC1}}$ and $\overline{\text{H\_OC2}}$ pins enables detection of the current value by sensing the voltage drop on Q1 and Q2 that are MOS transistors with very low switch-on resistance Rds(on). Q1 or Q2 is selected, depending on the desired maximum current value and this determines the value of Rds(on). For example, if the allowed maximum current is about 0.5 A, a voltage drop of 75 mV will trigger the overcurrent circuitry and an approximate value of Rds(on) = 150 MΩ will result. Connecting the ISP1160x input pins $\overline{\text{H\_OC1}}$ and $\overline{\text{H\_OC2}}$ to +5 V will disable the internal overcurrent protection of the ISP1160; an external overcurrent protection circuit may also be used.

The $\overline{\text{RESET}}$ input signal of the ISP1160x is connected to the RESET# input signal of the SPARClite processor, and both are connected to the system RESET generation circuitry.


+5V
+ C6
10uF/25V
C9
0.1uF
+3.3V
+ C5
10uF/25V
C8
0.1uF
+5V VDD +3.3V
JP4
1
2
3
HEADER 3
VDD
C3
0.1uF
VHOLD1
C4
0.1uF
IC1
CLK
154
CLKIN
153
CLKEXT
152
CLKSEL0
151
CLKSEL1
63
CLKSEL2
66
CTEST#
22
BTEST#
VCC
1K
R33
+5V
3.3V
+3.3V
+5V
GND
Fujitsu SPARClite
D0 43
D1 42
D2 41
D3 40
D4 37
D5 36
D6 35
D7 34
D8 32
D9 31
D10 30
D11 29
D12 27
D13 26
D14 25
D15 24
A1 91
A2 98
CS5# 80
RD/WR# 78
IRQ8 159
IRQ9 158
RESET# 148
READY# 110
D0 63
D1 64
D2 2
D3 3
D4 4
D5 5
D6 6
D7 7
D8 9
D9 10
D10 11
D11 12
D12 13
D13 14
D14 16
D15 17
A1
10K R205
CS_N
U3A
SN74LS14
INT1
VCC
10K R200
RESET_N
R22
10K
VCC
U1
VCC1 19
VCC2 56
Vreg 58
Vhold 24
H_WAKEUP 40
H_SUSPEND 42
TEST_LOW 37
n.c 36
NDP_SEL 33
H_PSW2_N 47
H_PSW1_N 46
H_OC2_N 55
H_OC1_N 54
H_D2+ 53
H_D2- 52
H_D1+ 51
H_D1- 50
TEST_LOW 49
TEST_LOW 48
n.c 38
TEST_LOW 39
n.c 41
X2 44
X1 43
GND1 1
GND2 8
GND3 15
GND4 18
GND8 62
GND7 57
GND6 45
GND5 35
A0
TEST_LOW 60
CS_N 21
RD_N 22
WR_N 23
DREQ1 25
n.c 26
DACK1 27
TEST_HIGH 28
EOT 34
INT1 29
n.c 30
n.c 31
RESET_N 32
R202
10K
R201
10K
R201
10K
VCC
H_PSW2_N
H_PSW1_N
H_OC2_N
H_OC1_N
VBUS_DN2
VBUS_DN1
H_D2+
H_D2-
H_D1+
H_D1-
10K R203
10K R204
10K R206
X2
XTAL1
6MHz
C1
27pF
C2
27pF
ISP1160_LQFP64
VREG
VHOLD2
C10
0.1uF
C7
0.1uF
+5V
VBUS_DN2
Q1
C21
0.1uF
VBUS_DN1
Q2
C22
0.1uF
VBUS_DN1
J5
VBUS 1
D- 2
D+ 3
GND 4
CHASSIS 5
USB_DOWN
R4 22
R5 22
H_D1-
H_D1+
C14 47pF
R6 15K
R7 15K
C15 47pF
VBUS_DN2
J6
VBUS 1
D- 2
D+ 3
GND 4
CHASSIS 5
USB_DOWN
R8 22
R9 22
H_D2-
H_D2+
C16 47pF
R10 15K
R11 15K
C17 47pF
Title
Size B
Number
Revision
Date: 16-Dec-2002
Sheet of
File: I:\Jason Backup 030701\Philips\ISP1161\Documentation\App Note Schematic\1160 sparclite.DDB

7. References

- *Universal Serial Bus Specification Rev. 2.0*
- *ISP1160 Embedded Universal Serial Bus Host Controller* datasheet
- *ISP1160A1 Embedded Universal Serial Bus Host Controller* datasheet
- *Interfacing ISP1160x to Hitachi SH7709 RISC Processor* Application Note.

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